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CLAIMS

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1. A branch predictor comprising:

branch prediction means for predicting a conditional branch of a branch instruction;

a comparator for generating a comparison signal by comparing the predicted conditional branch from the branch prediction means with a real conditional branch of the branch instruction;

an accuracy history table for storing an accuracy history of the predicted conditional branch;

a first state transition logic circuit for generating an accuracy history bit to be stored to the accuracy history table in response to the comparison signal; and

a multiplexer for outputting an alternative one of the conditional branch and an inverted conditional branch as a final branch prediction outcome, in response to a predicted accuracy history signal based on the accuracy history bit.

2. The branch predictor according to claim 1, wherein the branch prediction means comprises:

a branch history register for storing conditional branches of previous branch instructions;

a pattern history table for storing pattern history bits used for generating the predicted conditional branch corresponding to the conditional branches of the previous branch instructions stored in the branch history register; and

a second state transition logic circuit for generating the pattern history bits in response to the real conditional branch of the branch instruction.

3. The branch predictor according to claim 2, wherein the second state transition logic circuit includes an up/down saturating counter.

4. The branch predictor according to claim 1, wherein the accuracy history table includes a memory array.

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5. The branch predictor according to claim 1, wherein the comparator generates the comparison signal having a first logic value when the predicted conditional branch is the same as the real conditional branch, and generates the comparison signal having a second logic value when the predicted conditional branch is different from the real conditional branch.

6. The branch predictor according to claim 1, wherein the first state transition logic circuit includes an up/down saturating counter.

7. The branch predictor according to claim 6, wherein the first state transition logic circuit is used after learning the predicted branch accuracy of patterns of previous branch instructions.

8. The branch predictor according to claim 1, wherein the predicted accuracy signal is determined by a most significant bit of the accuracy history bit.